Broad Galaxy

PRELIMINARY

BG822CX DATASHEET

BROAD GALAXY

Preliminary Information
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BG822CX DATASHEET **1**

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PRELIMINARY

Chapter 1 Introduction

1.1 General Description

BG822CX is a high-IF transceiver specifically for GSM900, GSM1800, GSM1900, IS-95, SCDMA, PHS, TD-SCDMA and WCDMA. The receiver integrates all necessary modules including LNA, Mixer, VGA and LPF. The transmitter integrates the LPF, VGA, polyphase filter, modulator and output driver. Also VCOs and an integer-N PLL are fully on chip.

1.2 Features

- Flexible IF frequency selection
- Operating frequency band: 800 – 2200MHz
- Receiver: 50dB dynamic gain range, 1dB per step, ±0.5dB ripple
- Transmitter: 24dB dynamic gain range, 1dB per step, ±0.5dB ripple
- Fully Integrated VCOs and an integer-N PLL
- On-chip 4th order low pass filter for receiver
- Differential design minimizing cross-talk and spurs
- Common 3 wire serial bus interface

1.3 Applications

- In-building coverage for wireless communications
- Mobile terminals
- Satellite communications

1.4 Block Diagram

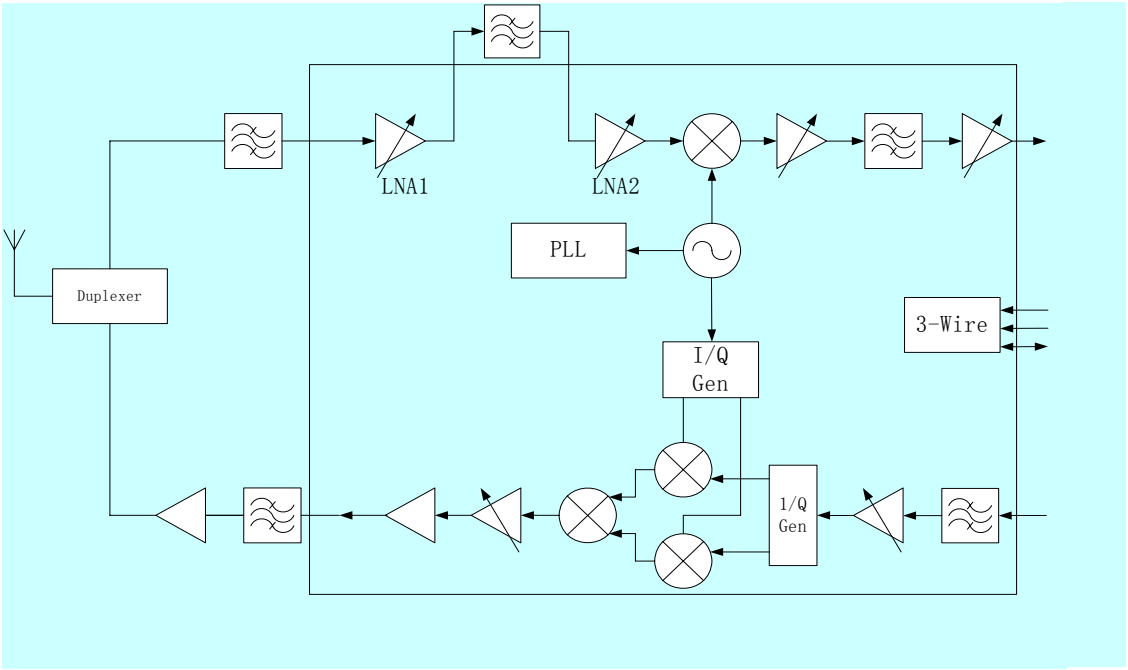

Fig. 1 MPWC transceiver block diagram

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1.5 Pin Configuration

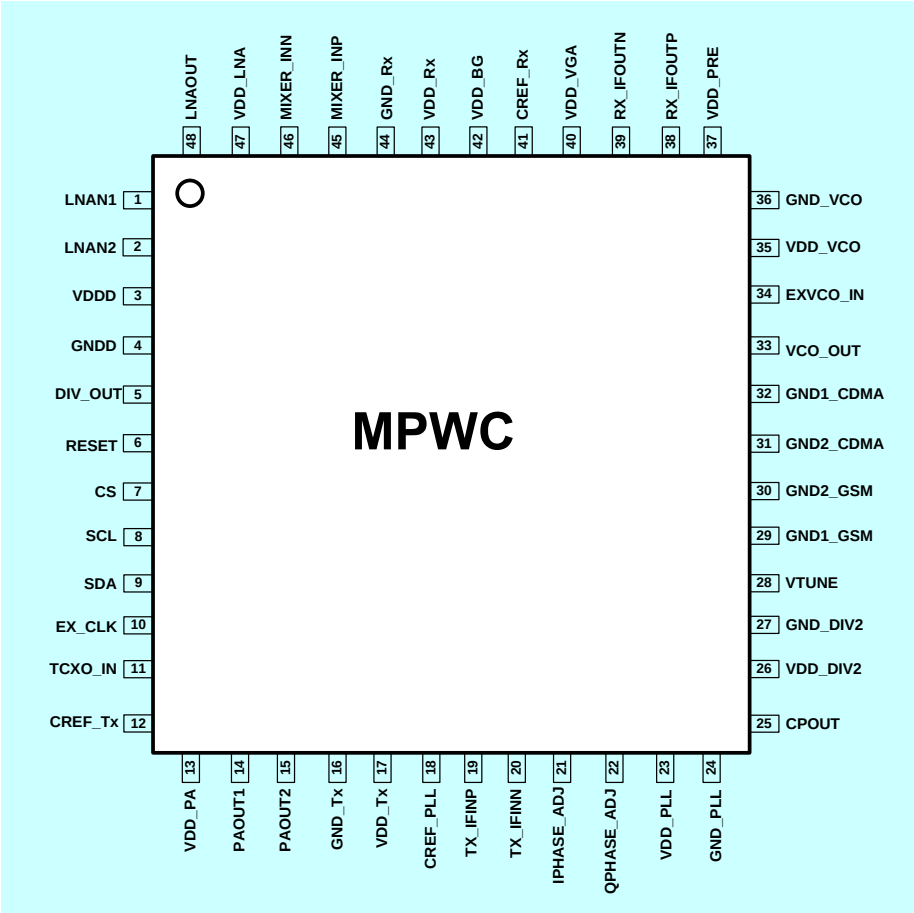

Fig. 2 Pin configuration

1.6 Pin Descriptions

Pin Number	Name	I/O	Description
1	LNAIN1	I	1800MHz band RF input
2	LNAIN2	I	900MHz band RF input
3	VDDD		Power supply of the digital part
4	GNDD		Ground of the digital part
5	DIV_OUT	O	PLL divider output for testing
6	RESET	I	Reset for the digital part, normal low logic.
7	CS	I	3-wire serial-interface enable input.
8	SCL	I	3-wire serial-interface clock input.
9	SDA	I/O	3-wire serial-interface data input/output.
10	EX_CLK	O	TCXO clock formed output for testing.
11	TCXO_IN	I	TCXO input
12	CREF_Tx	O	Voltage reference output for the Tx chain

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13	VDD_PA		Power supply of PA driver part
14	PAOUT1	O	900MHz band PA output
15	PAOUT2	O	1800MHz band PA output
16	GND_Tx		Ground of the Tx chain
17	VDD_Tx		Power supply of the Tx chain
18	CREF_PLL	O	Voltage reference output for the PLL part
19	TX_IFINP	I	Base band positive input
20	TX_IFINN	I	Base band negative input
21	IPHASE_ADJ	I	I-phase adjustment input
22	QPHASE_ADJ	I	Q-phase adjustment input
23	VDD_PLL		Power supply of the PLL
24	GND_PLL		Ground of the PLL
25	CPOUT	O	Charge pump current output
26	VDD_DIV		Power supply of the Divider part
27	GND_DIV		Ground of the Divider part
28	VTUNE	I	VCO tune voltage input
29	GND1_GSM		Ground 1 of GSM VCO
30	GND2_GSM		Ground 2 of GSM VCO
31	GND2_CDMA		Ground 2 of CDMA VCO
32	GND1_CDMA		Ground 1 of CDMA VCO
33	VCO_OUT	O	VCO output for testing
34	EXVCO_IN	I	External VCO input for testing
35	VDD_VCO		Power supply of the VCO part
36	GND_VCO		Ground of the VCO part
37	VDD_PRE		Power supply of the Prescaler part
38	RX_IFOUTP	I	RX IF positive output
39	RX_IFOUTN	I	RX IF negative output
40	VDD_VGA		Power supply of the VGA part
41	CREF_Rx	O	Voltage reference output for the Rx chain
42	VDD_BG		Power supply of the Rx Bandgap part
43	VDD_Rx		Power supply of the Rx chain
44	GND_Rx		Ground of the Rx chain
45	MIXER_INP	I	RX MIXER positive input
46	MIXER_INN	I	RX MIXER negative input
47	VDD_LNA		Power supply of the LNA part
48	LNAOUT	O	LNA output

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Chapter 2 Functional Description

2.1 Receiver

The receiver consists of LNA1, LNA2 and RF mixer, AGC, and low pass filter (RX LPF).The RF signal is fed from antenna, through the RF filter and connected to the input of LNA1 then goes to the RF mixer which converts the RF signal down to a high IF frequency . In order to maintain the IF output level for cable transmission, the internal IF AGC can offer gain control capability.

a) LNA1

LNA1 is integrated on chip. The first one is around 900MHz, which is designed for IS-95 and GSM900 receivers. The second one is around 2000MHz, which is designed for GSM1800, GSM1900, SCDMA, PHS, WCDMA and TD-SCDMA. LNA1 is the first block in receiver. Its function is to provide enough gain to overcome the noise of subsequent stages. LNA1 can be set into three modes: bypass mode, low gain mode and high gain mode via the control software using the 3-wire bus serial programming. Both the input and output of LNA1 are single-ended 50 ohm. The dual-band LNA1 covers a wideband frequency band from 800MHz to 2200MHz：

IS-95：824MHz~869MHz;
GSM900：890MHz~915MHz;
GSM1800：1710MHz~1785MHz;
GSM1900：1850~1910MHz;
SCDMA：1785.25MHz~1804.75MHz;
PHS：1891.15MHz~1917.95MHz;
WCDMA：1920MHz~1980MHz;
TD-SCDMA：2010-2025MHz.

b) LNA2+MIXER

There are two LNA2+Mixer on chip covering two frequency bands respectively. The first one is working at 900MHz, which is designed for IS-95 and GSM900 receivers. The second one is working at 2000MHz, designed for GSM1800, GSM1900, SCDMA, PHS, WCDMA and TD-SCDMA receivers. Both the LNA2+Mixer can be set into two modes, low gain mode and high gain mode via the control software using the 3-wire bus serial programming. The external input matching circuit is needed to connect with external RF filter or Balun.

c) VGA and LPF

The receiver channel filter is a 4-pole low pass filter giving the necessary blocking filtering. The filter can be easily configured to be 60MHz, 100MHz and 120MHz by 3-wire serial bus.

The VGAs, both RX VGA and TX VGA, are linear-in-dB and usable at frequencies from 40 MHz to 120 MHz. Over the whole frequency range, the gain variation is less than 1 dB.

In RX VGA, there is a DC offset adjustment circuit which controls the IF output DC voltage.

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With this circuit, the DC level can be adjusted from -6 mV to +8 mV off the nominal value. RX The VGA is supposed to drive an output load of 100 Ohm at 1V Vp-p differential Output Level.

2.2 Transmitter

Analog IF signals are fed to transmission path, and modulated to RF signal, then goes to antenna through PA, filter and antenna switch. The transmitter consists of TX LPF, VGA ,RF Mixer and RF driver which connects to the external band-pass filter and PA.

a) Transmitter Low Pass Filter, VGA

The IF signals from the cable are sent to the low pass filter with high order harmonics suppression. To compensate the loss of the cable, a VGA at IF frequency is needed. The TX VGA has a gain range of 16 dB with 1 dB gain step.
The filter achieves a 60MHz/90MHz/120 MHz programmable cutoff frequencies with 2 bits digital control word. The low pass filter is an active RC 4^{th} order filter. One important parameter for the filter is the accuracy of the 3dB Cut-off frequency. In order to achieve this performance we use a 2 bits digital control word that adjusts the capacitor to correct process and temperature drift.

b) RF Mixer (Up Converter)

To get sideband rejection, a polyphase filter is applied in the IF channel. The up-conversion mixers are used to mix up the IF signals to a RF signal. The mixer and the IF polyphase filter suppresses the sideband.

The Up-converter combined with a polyphase filter achieves -35dBc sideband rejection and -27dBc LO leakage rejection at the output of the TX (transmission) chain.
Both of the two mixers are designed for wideband application. The input signal frequency of down-converter is from 800 to 2200 MHz and the output IF frequency is from 40 to 120MHz.

c) RF Variable Gain Amplifier and PA driver (RF VGA+Driver)

Two PA Drivers are integrated on chip. The first one is around 900MHz, for covering IS-95 and GSM900 bands. The second one is around 2000MHz to cover GSM1800, GSM1900, SCDMA, TD-SCDMA, WCDMA and PHS bands. The RF VGA offers 9dB gain control range. To improve 1dB compression point, the PA buffer is an open collector output. Pull-up inductor and matching network is needed. The output driver is single-ended and easily to be matched to the commonly used RF filters.
The Pre-PA is the last stage of the transmitter. It consists of three blocks, RF-VGA, Differential to Single amplifier, and PA-driver. The RF-VGA, provides the 18dB or 27dB output voltage gain. The Pre-PA includes two sub- PA-drivers, one works at 820MHz to 960MHz, and the other works at the other frequency band.

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2.3 Synthesizer

RF frequency synthesizer provides the local oscillator signal to the transceiver. The chip integrates all the components of the synthesizer, including VCO, integer-N divider, F/P detector, charge pump and other control circuit. Only the loop low pass filter is external. Channel is controlled by 3 wire SPI bus. The fast-lock circuit is used to speed up the synthesizer settling-time.

2.4 3-wire section

3-wire is used to communicate with other controllers. Timing diagram is shown as the following.

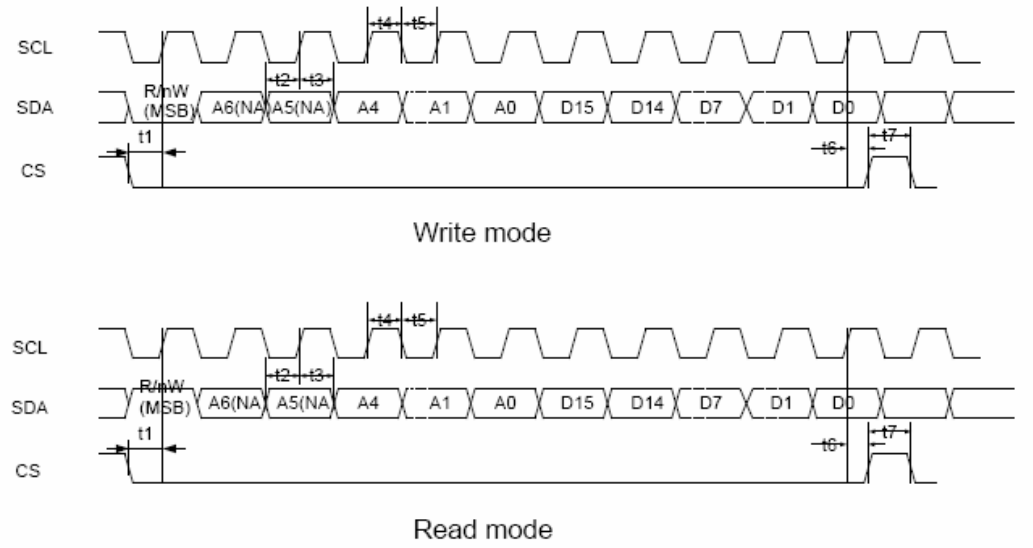

Fig. 3 SPI timing diagram

Table 3 SPI timing specifications

Parameter	Description	Min	Typ	Max	Unit
t1	CS setup time	20			nS
t2	SDA to SCL setup time	20			nS
t3	SDA to SCL hold time	20			nS
t4	SCL high duration	50			nS
t5	SCL low duration	50			nS
t6	SCL to CS setup time	20			nS
t7	CS pulse width	100			nS

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Chapter 3 Electrical Characteristics

Parameter	Description	Min.	Typ.	Max.	Unit
Receive					
$f_{RF,RX}$	Rx input frequency range				MHz
	IS-95	824		849	
	GSM900	890		915	
	GSM1800	1710		1785	
	GSM1900	1850		1910	
	SCDMA	1785.25		1804.75	
	PHS	1891.15		1917.95	
	WCDMA	1920		1980	
	TD-SCDMA	2010		2025	
F_{IF}	IF frequency	40		120	MHz
NF	Noise figure		4	5	dB
$G_{RX,voltage}$	RX channel total voltage gain	48		100	dB
G_{vSTEP}	AGC gain step		1		dB
$BW_{1dB,LPF}$	IF LPF 1dB bandwidth				MHz
	Mode 1		120		
	Mode 2		100		
	Mode 3		60		
Transmit					
$f_{RF,TX}$	Tx output frequency range				MHz
	IS-95	869		894	
	GSM900	935		960	
	GSM1800	1805		1880	
	GSM1900	1930		1990	
	SCDMA	1785.25		1804.75	
	PHS	1891.15		1917.95	
	TD-SCDMA	2010		2025	
	WCDMA	2110		2170	
$Z_{TX,out}$	Matched load (single-ended)		50		Ohm
$P_{OUT,max}$	Maximum Linearity Output power		4		dBm
P_{off}	Transmitter off power		-100		dBm
ΔPVGC	VGC tuning range		24		dB
GP STEP	VGC gain step		1		dB
Glinear	VGC gain control linearity- within any 20 dB gain range in board at any temperature	-1 -3		+1 +3	dB
$REJ_{sideband}$	Sideband rejection		-35		dBc

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Parameter	Description	Min.	Typ.	Max.	Unit
$P_{leakage}$	LO leakage rejection			-27	dBc
EVM	Modulate at WCDMA @ full power output		5		%
Synthesize					
f_{VCO}	Frequency Range of VCO	1648		4340	MHz
YN_{PN}	Synthesizer Phase noise				dBc/Hz
	GSM900,GSM1800,GSM1900,SCDMA ,PHS,				
	WCDMA and TD-SCDMA mode				
	@ 100 Hz offset		-60		
	@ 1 kHz offset		-78		
	@ 10 kHz offset		-81		
	@ 100 kHz offset		-91		
	@ 1 MHz offset		-122		
	@ ≥10 MHz offset		-142		
	IS-95 modes				
	@ 100 Hz offset		-50		
	@ 1 kHz offset		-68		
	@ 10 kHz offset		-69		
	@ 100 kHz offset		-98		
	@ 1 MHz offset		-123		
	@ ≥10 MHz offset		-142		
t_{lock}	Lock Time(frequency error < 1kHz)				usec
	IS-95		400		
	GSM900		200		
	GSM1800		200		
	GSM1900		200		
	SCDMA		200		
	PHS		200		
	TD-SCDMA		200		
	WCDMA		200		
BW_{loop}	Loop bandwidth				kHz
	IS-95		10		
	GSM900		40		
	GSM1800		40		
	GSM1900		40		
	SCDMA		50		
	PHS		60		
	TD-SCDMA		40		
	WCDMA		40		
Fref					
f_{REF}	Reference frequency		12		MHz
V_{REF}	input voltage level	800		1000	mV
R_{IN}	Input resistance @12MHz		10K		Ohm

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Parameter	Description	Min.	Typ.	Max.	Unit
C_{IN}	Input capacitance		1		pF

Chapter 4 Application Information

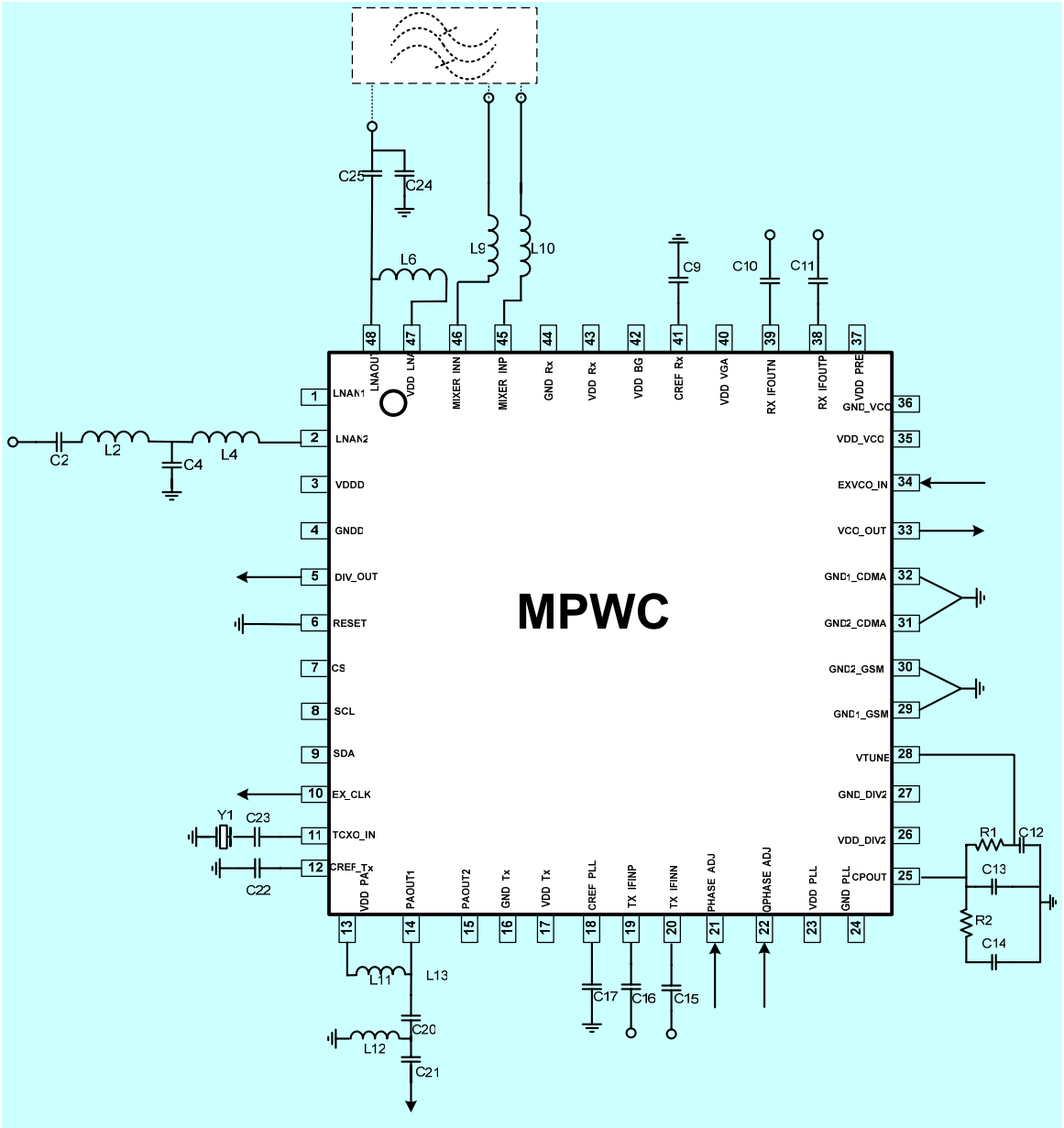

Fig. 4 900MHz band application circuit

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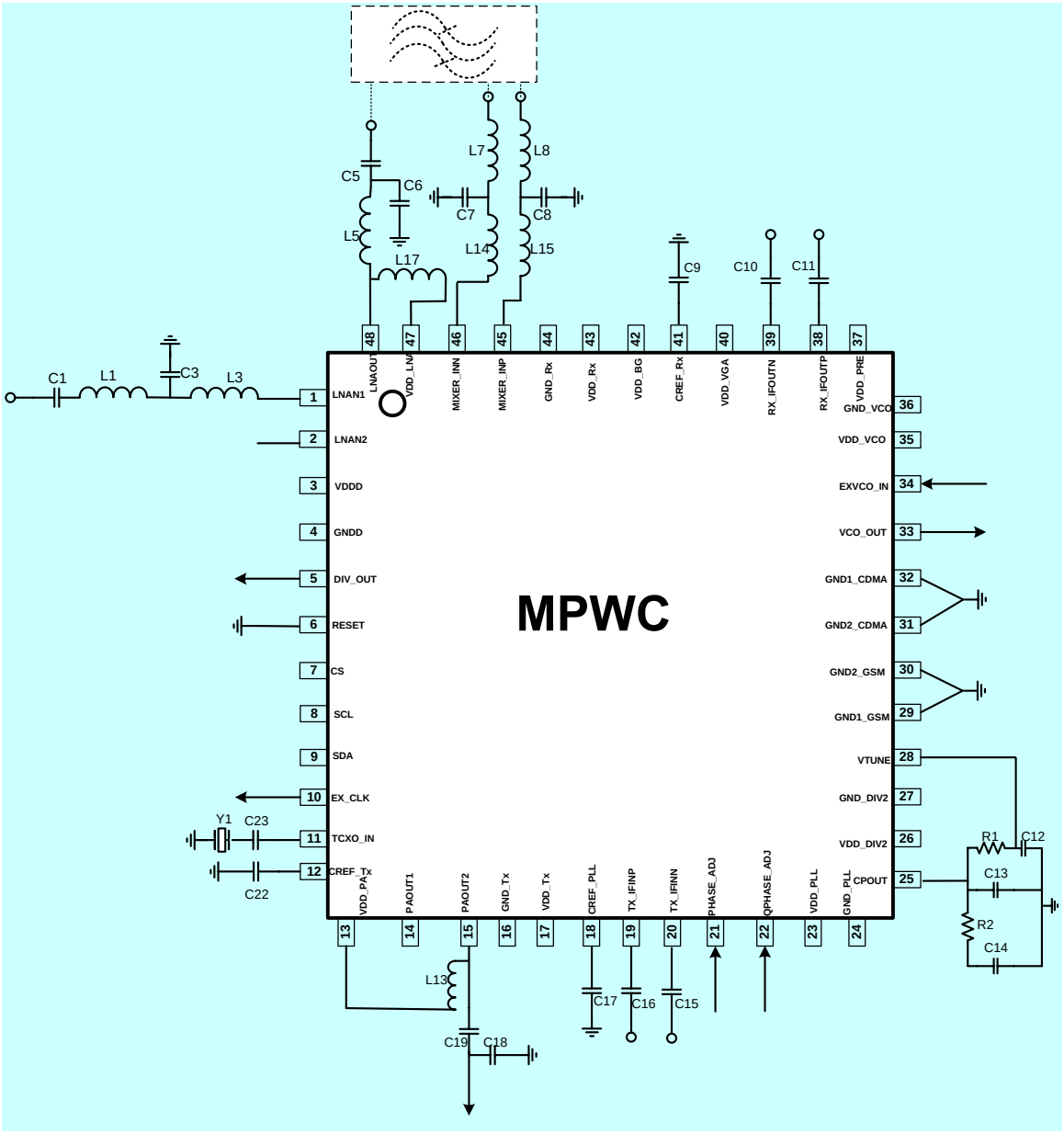

Fig. 5 1900MHz band application circuit

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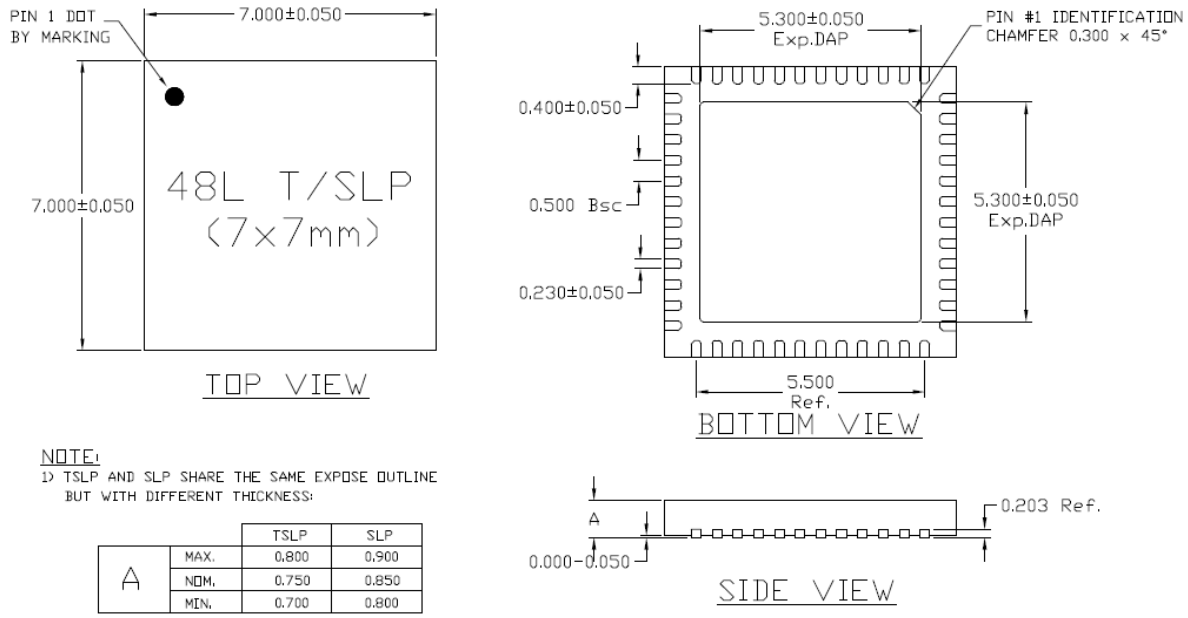
Device	Value	Device	Value	Device	Value
C1, C2	5pF	L1	1nH	R1	1.6k
C3, C7, C8	1pF	L2	4.7nH	R2	510
C4	2pF	L3	3.6nH		
C5, C6	1.8pF	L4	6.2nH		
C9, C17, C22	100pF	L5	1nH		
C10, C11, C15, C16, C23	1nF	L6	6.2nH		
C18	1pF	L7, L8	3.3nH		
C19	2pF	L9, L10	10nH		
C20	2pF	L11	24nnH		
C12	4.7nF	L12	15nH		
C13	10nF	L13	4.7nH		
C14	100nF	L14, L15	8.2nH		

Table 1 the application circuit LC reference value

Package Outline

QFN48



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