ALTERA®

Stratix III FPGAs

Bring your ideas to life.

It's a jungle out there. Give your ideas life with a device that puts your designs at the top of the food chain. Cheetah-like speed, elephant-sized memory, and power that adapts to performance like a chameleon to its environment.

Rule the jungle with Altera's Stratix III FPGAs. After all, natural selection doesn't just apply to nature.

agile and cool

Rule the jungle with confidence

High-end designs are getting more complex—and the competition is getting fierce in your rapidly changing marketplace. To stay at the top of the food chain, you need a solution that addresses all your design and business challenges, anticipates the unforeseen, and helps you win in your market.

Altera's Stratix® III FPGAs are designed precisely to help you to do all this and more. We're addressing your applications' increased levels of integration and complexity with higher densities and performance, while decreasing power consumption. At the same time our development tools provide the industry's highest productivity. With Stratix III FPGAs, you can design with confidence.

To meet diverse application needs, Altera offers three Stratix III family variants:

Stratix III L FPGAs deliver balanced logic, memory, and DSP resources for general-purpose applications

Stratix III E FPGAs provide enhanced memory and DSP resources for memory- and DSP-intensive applications

Stratix III GX FPGAs offer integrated transceivers for high-bandwidth interface applications

The foundation for your next design

The Stratix III family's advanced features boost the functionality of your high-performance systems, giving you an edge over your competition.

While designing with Stratix III FPGAs, you'll experience the industry's highest productivity and performance benefits with our Quartus® II software. Quartus II software incorporates embedded and DSP system integration tools, incremental compilation, power optimization, and even board planning so you can finish your designs faster. In addition, Quartus II software works seamlessly with third-party tools.

To help you take advantage of advanced Stratix III features and to get to market faster, we also offer flexible, optimized, pre-packaged intellectual property (IP) cores for common system and connectivity functions.

And when you're ready to move to high volume, we have the industry's only risk-free path from a high-end FPGA to high-volume structured ASICs. HardCopy® structured ASICs give you the most cost-effective solution for high-volume production requirements.

By choosing Altera as your FPGA supplier, you can be confident that you're choosing a partner who you can trust every step of the way, from prototype to production, with the industry's best track record of delivering high-quality products on schedule and in volume.

Extending performance leadership

Altera continues to lead the industry in performance with the Stratix III family.

- 25 percent higher performance over previous-generation devices
- At least one speed grade faster than the nearest competing devices
- Internal clock speed of up to 600 MHz
- Quartus II software with the ASIC-strength TimeQuest timing analysis tool maximizes performance.
- Migrating your design to HardCopy structured ASICs allows further performance enhancements.

Minimize your design's power consumption

Meet your design specs and keep power under control with our suite of low-power features.

Programmable Power Technology

Programmable Power Technology uses your design information to minimize power consumption for every programmable logic array block (LAB), DSP block, and memory block. Quartus II software automatically analyzes your design and identifies the performance needs of each block. While most logic, including unused logic, is set to a new low-power mode, the high-performance, timing-critical blocks are set to high-speed mode. Programmable Power Technology ensures the highest performance and lowest power consumption possible for your design.

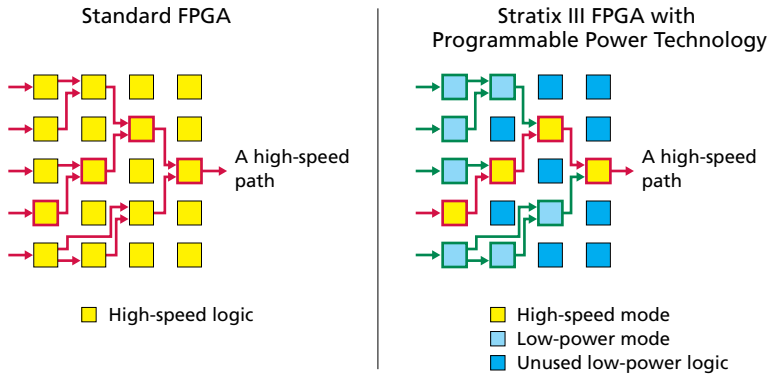
Selectable core voltage

Selectable core voltage, another Stratix III power feature, gives you the option of using either 1.1-V or 0.9-V core voltage. Designs needing the highest performance use the 1.1-V core voltage, while designs requiring minimum power consumption can choose to use the 0.9-V core voltage.

Quartus II PowerPlay power optimization

The Quartus II PowerPlay power optimization tool keeps total power to a minimum. Since 2005, we've offered advanced power optimization capabilities in our Quartus II software, and its value was proven in our customers' designs—contributing to an average 25 percent reduction in dynamic power. Since then, we've continued to improve PowerPlay, adding intelligent decision making in synthesis, placement, and routing. PowerPlay also provides accurate power estimation early in the design process, detailed power analysis reports, and an automated power advisor. Working together with Programmable Power Technology in the Stratix III silicon, PowerPlay keeps your design's power consumption to a minimum.

Standard FPGA logic vs. Stratix III FPGA logic



Programmable Power Technology gives you ***maximum performance*** *where you need it and the* ***lowest power*** *everywhere else.*

Stratix III architecture

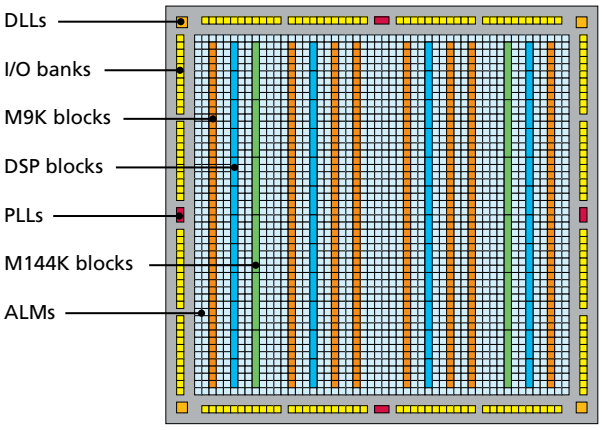
Based on the successful Stratix II architecture, we built Stratix III FPGAs to address your high-end system requirements. Stratix III devices include adaptive logic modules (ALMs) and high-performance, flexible memory and DSP blocks to meet your system's most demanding requirements. The I/O banks and external memory interfaces make designing your boards easier, and design security features keep your designs secure.

Stratix III features include:

- Up to 340K equivalent logic elements, 17 Mbits of memory, and 576 multipliers in the L variant—for the industry's biggest FPGAs
- 25 percent higher performance and 50 percent lower power than prior-generation FPGAs
- Up to 896 18-bit x 18-bit multipliers operating at 550 MHz in the E variant
- Up to 24 high-performance I/O banks
- Best-in-class signal integrity

industry's ***largest*** *FPGAs*

Stratix III E EP3SE50 floorplan



Flexible, efficient ALMs

Stratix III devices are based on the innovative adaptive logic modules that Altera introduced in 2004 with Stratix II FPGAs. ALMs are based on our patented eight-input "fracturable" look-up table (LUT) with two dedicated adders and two registers.

Fracturable LUTs allow ALMs to pack more functionality into the same amount of logic. ALMs can implement six-input functions, some seven-input functions, or multiple other combinations of functions with varying numbers of inputs. ALMs are the basis of the industry's most efficient and highest-performance logic architecture.

ALM details:

- 2:1 register-to-LUT ratio in ALMs ensures that the FPGA is not register-limited for register-rich designs.
- For DSP applications, ALMs include two dedicated adders capable of two-bit additions, or a single ternary adder for advanced arithmetic computations.
- Ten ALMs in a single LAB can be converted into a 640-bit MLAB memory block to get more data ports for greater memory bandwidth.

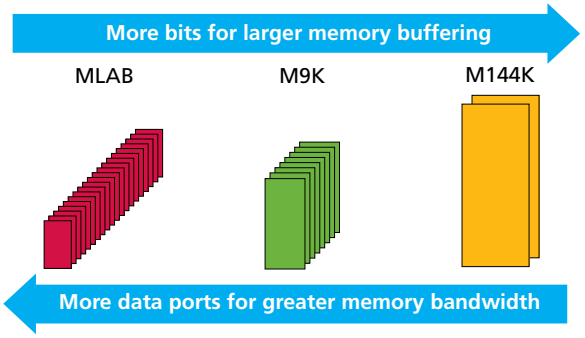
TriMatrix memory for the perfect fit

TriMatrix memory is more flexible and efficient and provides higher memory bandwidth than any other FPGA memory architecture. Stratix III TriMatrix memory includes three sizes of memory blocks: MLAB blocks, M9K blocks, and M144K blocks.

TriMatrix memory details:

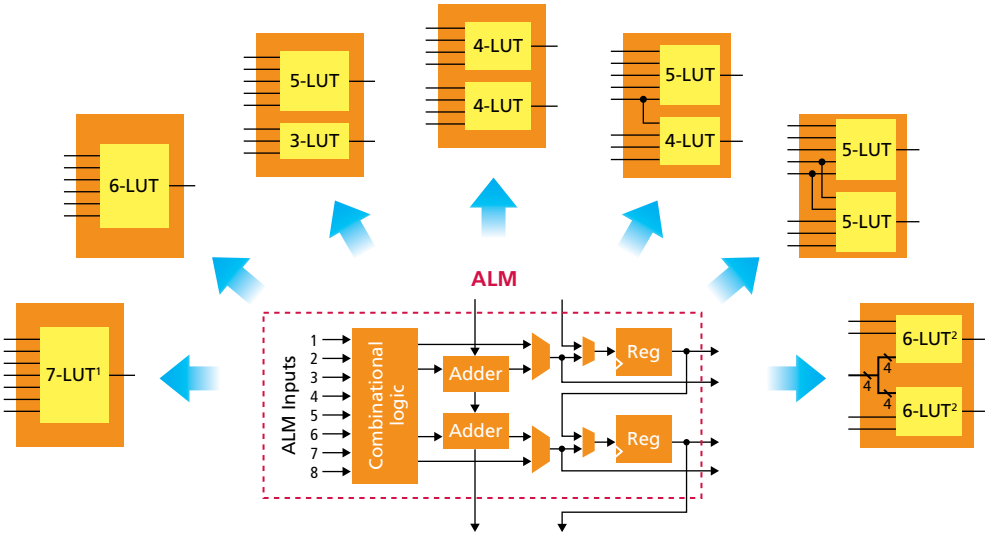
- Provides up to 17 Mbits of memory performing at over 600 MHz
- Includes features such as dual-port RAM mode, error correction coding (ECC), and low-power mode
- Stratix III E devices include the most memory and DSP blocks for memory-intensive applications.

TriMatrix memory



MLAB	M9K	M144K
• 640 bits per block • Up to 6,750 blocks • Shift registers, small FIFO buffers, filter delay lines	• 9,216 bits per block • Up to 1,144 blocks • General-purpose applications, packet headers, cell buffers	• 147,456 bits per block • Up to 48 blocks • Processor code storage, packet or video frame buffers

ALM block diagram and example LUT configurations



Notes: [1] Stratix III ALM can implement a subset of 7-input functions
[2] Must have the same logical function

Highest-performance digital signal processing

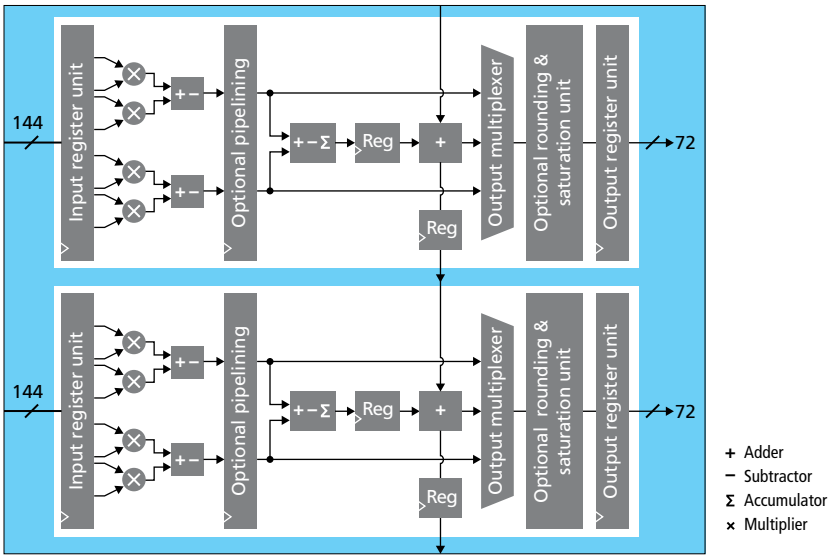
For the highest-performance, most silicon-efficient programmable DSP functions, Stratix III FPGAs include DSP blocks with twice the multiplier capabilities of competing devices. These DSP blocks deliver up to 60 times more multiplier/accumulator processing performance than the industry's highest-performance DSP processors with lower power, lower cost, and smaller board space for equivalent processing capability. For DSP-intensive applications, the Stratix III E devices include the most DSP and memory blocks in the family.

In addition, we provide application-optimized IP (such as our Nios® II embedded processors and DSP IP) and development tools (DSP Builder, SOPC Builder, and C2H Compiler) to make your video and imaging, baseband, intermediate frequency, and encryption applications easier to design.

DSP block details:

- Variable bit-width multipliers, adders/accumulators, pipeline registers, and other arithmetic operations
- Up to 896 18-bit x 18-bit multipliers capable of operating at up to 550 MHz

DSP block



High-performance external memory interfaces

Stratix III I/O banks support existing and emerging high-performance external memory standards. Our free self-calibrating soft IP core takes advantage of Stratix III I/O features and, along with the Quartus II TimeQuest timing analysis tool, provides a total solution for reliable high-frequency operation across process, voltage, and temperature (PVT).

Flexible I/O banks

Stratix III I/O banks give you high performance, high flexibility, and superior signal integrity when using multiple I/O standards and voltages. These modular I/O banks simplify your board layout and device migration while giving your design greater pin efficiency.

I/O bank details:

- Supports over 40 I/O standards
- Up to 24 independent banks per device
- LVDS operation and DQ/DQS pins supported on all I/O banks
- Timing analysis, pin planning, and signal integrity tools provide ease-of-use and rapid integration.

I/O banks

Best-in-class differential signaling support

- Up to 132 full-duplex 1.25-Gbps LVDS channels (132 transmit and 132 receive)
- Hard dynamic phase alignment (DPA) block with SERDES and clock forwarding capability for soft clock-data recovery (CDR)
- Programmable pre-emphasis and programmable voltage output differential (V_{OD})
- Calibrated differential on-chip termination

Best-in-class single-ended I/O support

- Programmable slew rate and drive strength
- Calibrated serial, parallel, and dynamic on-chip termination
- Programmable trace-length mismatch compensation

Best-in-class signal integrity

- 8:1:1 user I/O to power/ground ratio
- On-die and on-package decoupling

Stratix III external memory interfaces

Memory standard	I/O standard	Maximum clock speed (MHz)	Maximum data rate (Mbps)
DDR SDRAM	SSTL-2	200	400
DDR2 SDRAM	SSTL-1.8	400	800
DDR3	SSTL-1.5	400	800
QDRII	1.8-V/1.5-V HSTL	350	1,400
QDRII +	1.8-V/1.5-V HSTL	350	1,400
RLDRAMII	1.8-V HSTL	400	800

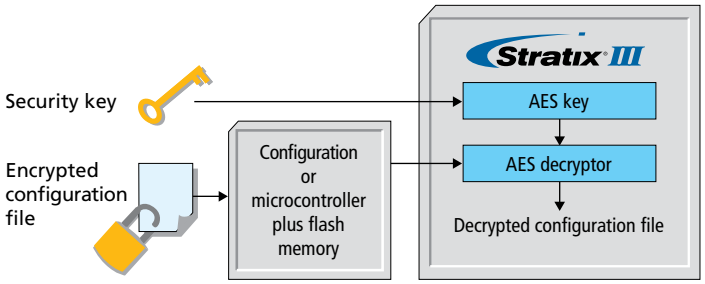
Built-in design security

To protect your designs against copying, reverse engineering, and tampering, Stratix III FPGAs feature built-in configuration bit-stream encryption.

Design security details:

- AES encryption with FIPS-197 certification
- 256-bit key length
- Industry's only design security solution with both volatile and non-volatile key options. The volatile key is reprogrammable, and the non-volatile key is more practical, easy to use and low cost.
- Support for a variety of applications, including military anti-tampering and IP protection for ASSP and IP vendors.

Design security



Stratix III family details

Overview

Stratix III variant[1]	Device	ALMs	Equivalent LEs	Registers[2]	M9K blocks	M144K blocks	Embedded memory (bits)	MLAB (bits)	Maximum 18-bit x 18-bit multipliers
Stratix III L (Logic)	EP3SL50	19,000	47,500	38,000	108	6	1.8M	0.6M	216
	EP3SL70	27,000	67,500	54,000	150	6	2.2M	0.9M	288
	EP3SL110	42,600	106,500	85,200	275	12	4.2M	1.3M	288
	EP3SL150	56,800	142,000	113,600	355	16	5.5M	1.8M	384
	EP3SL200	79,560	198,900	159,120	468	24	7.7M	2.5M	576
	EP3SE260[3]	101,760	254,400	203,520	864	48	14.6M	3.2M	768
	EP3SL340	135,200	338,000	270,400	1,144	48	17.2M	4.2M	576
Stratix III E (Enhanced)	EP3SE50	19,000	47,500	38,000	400	12	5.3M	0.6M	384
	EP3SE80	32,000	80,000	64,000	495	12	6.2M	1.0M	672
	EP3SE110	42,600	106,500	85,200	639	16	8.0M	1.3M	896
	EP3SE260[3]	101,760	254,400	203,520	864	48	14.6M	3.2M	768

Notes: [1] For Stratix III GX details, please contact your sales representative.
[2] This is the base core logic register count. An ALM can support three registers when used in LUTREG mode, which can increase the total register count by 50 percent.
[3] EP3SE260 FPGAs are the optimum solution for both logic (Stratix III L) and DSP/memory (Stratix III E) applications at this density.

Packaging

Stratix III variant	Device	484-pin FBGA*	780-pin FBGA*	1,152-pin FBGA*	1,517-pin FBGA*	1,760-pin FBGA*
Stratix III L (Logic)	EP3SL50, EP3SL70	288	480			
	EP3SL110, EP3SL150		480	736		
	EP3SL200			736	864	
	EP3SE260			736	960	
	EP3SL340				960	1,104
Stratix III E (Enhanced)	EP3SE50	288	480			
	EP3SE80, EP3SE110		480	736		
	EP3SE260			736	960	

288 Number indicates available user I/O pins

Vertical migration (same V_{CC}, GND, ISP, and input pins)

All Stratix series devices are offered in commercial and industrial temperatures and lead-free packages.

*FBGA: FineLine BGA (FlipChip)

Easy migration to low-cost, high-volume production

After you've developed your design and tested it in-system, we offer migration to lower-cost and lower-power HardCopy structured ASICs for high-volume production. Because HardCopy devices are functionally equivalent to the FPGA, we guarantee delivery of socket-compatible silicon based on the FPGA prototype, with minimal effort on your part. Altera is the only supplier able to offer this guaranteed, low-risk path to low-cost volume production.

Maximize productivity with Quartus II software

Silicon alone is nothing without easy-to-use software. Quartus II software delivers the industry's highest productivity and performance features for the smoothest design process.

Using Quartus II software, you'll exceed your performance goals, complete your design faster, and meet power budgets for your Stratix III designs. Advanced place-and-route technology, physical synthesis, and the TimeQuest timing analyzer help you close timing—fast. Using the industry's first and most comprehensive incremental compilation feature, you'll reduce your design cycle with shorter compile times and more design iterations. Finally, PowerPlay power analysis and optimization technology will automatically minimize your design's power consumption.

Simple system integration

You can implement an entire system on Stratix III FPGAs to lower your costs, achieve higher performance, increase flexibility, and reduce your design time—and Quartus II software makes that system integration easier.

Our industry-leading embedded and DSP system design tools, including SOPC Builder, C2H Compiler, and DSP Builder, automate your system design from front to back. With these tools, you can include a wide array of IP cores (including the Nios II embedded processor, memory controllers, interface controllers, and a variety of application-specific cores), customize them to your application, and connect them—automatically generating hardware, software, and simulation models for your custom application.

Convenient training

Whether you're an experienced FPGA designer or new to FPGAs, our online or instructor-led training can help you get your design started. These courses teach you the most efficient FPGA design techniques, how to create high-quality Stratix III systems, and tips to get your product to market as fast as possible.

Design with confidence

Altera is committed to your success. Our operational excellence results in world-class quality and delivery of leading-edge programmable logic technology. Our history of on-time new product rollouts, including the Stratix, Stratix II, and Stratix II GX FPGAs, can give you confidence that when you're ready to go to production, we'll be there with you.

*"One significant factor in our selection of Stratix II GX FPGAs for our products was **Altera's solid operational track record** of delivering functional devices on time and as promised. Stratix II GX devices provide data rates of over 4 Gbps per channel in our systems, enabling our products to shorten image-generation time without compromising diagnostic detail, and **helping us to maintain our worldwide leadership** in medical imaging."*

— Stefan Pflaum
Head of Research and Development
Computed Tomography, SIEMENS AG

Take the next step

Visit **www.altera.com/stratix3** to read detailed product information, view net seminars and online demos, find sales and distributor contacts, and more. You can also download Quartus II software to design Stratix III FPGAs.

Start your next successful design today!

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